Amendments to the Claims

1. (CURRENTLY AMENDED) A semiconductor device having a semiconductor body ~~(22)~~ comprising an active area ~~(7)~~ and a termination structure ~~(16)~~ surrounding the active area, the termination structure comprising a plurality of lateral trenchgate transistor devices ~~(2a-to-2d)~~ connected in series and extending from the active area towards a peripheral edge ~~(42)~~ of the semiconductor body, each lateral device comprising a trench ~~(30)~~ having a gate electrode ~~(31)~~ therein separated from the semiconductor body by a layer ~~(32)~~ of gate insulating material, the trenches, gate electrodes and layers of gate insulating material of the lateral devices being formed in the same respective process steps as trenches ~~(20)~~, insulated electrodes ~~(11)~~ therein and layers ~~(25)~~ of material insulating the insulated electrodes of devices in the active area, the gate electrodes ~~(31)~~ of the lateral devices extending through a region ~~(15)~~ of a first conductivity type, and part way through an underlying region ~~(14a)~~ of a second, opposite conductivity type, with each lateral device including an electrically conductive connection ~~(8,23)~~ between its gate electrode ~~(31)~~ and the first conductivity type region ~~(15)~~ at the side of the lateral device closer to the active area, such that a voltage difference between the active area and the peripheral edge is distributed across the lateral devices.

2. (CURRENTLY AMENDED) A semiconductor device of Claim 1 wherein the active area ~~(7)~~ comprises devices having a region ~~(15)~~ of the first conductivity type which is formed in the same process step as the first conductivity type region ~~(15)~~ of the lateral devices.

3. (CURRENTLY AMENDED) A semiconductor device of ~~Claim 1 or Claim 2~~Claim 1 wherein the insulated electrodes of the active area devices are gate electrodes ~~(11)~~ of trench-gate transistor devices, and the first conductivity type region of the active area devices forms a channel-accommodating region ~~(15)~~ thereof.

4. (CURRENTLY AMENDED) A semiconductor device of ~~Claim 1 or Claim 2~~ Claim 1 wherein the

insulated electrodes of the active area devices are trenched electrodes ~~(60)~~ of Schottky rectifiers.

5. (CURRENTLY AMENDED) A semiconductor device of ~~any preceding Claim~~ Claim 1 wherein the layer of insulating material ~~(32)~~ is thicker over the bottom of the trenches ~~(30)~~ of the lateral devices ~~(2a-to-2d)~~ than over at least a

portion of the sidewalls of said trenches.

6. (CURRENTLY AMENDED) A semiconductor device of ~~any preceding Claim~~ Claim 1 wherein the doping level of a respective portion ~~(50)~~ of the region ~~(14a)~~ of second conductivity type adjacent the bottom of each of the gate trenches ~~(30)~~ of the lateral devices is higher than that of the remainder of the second conductivity type region.

7. (CURRENTLY AMENDED) A semiconductor device of ~~any preceding Claim~~ Claim 1 wherein the semiconductor body ~~(22)~~ is rectangular in the plane of the body, and the connections ~~(8,23)~~ are provided towards one or more corners of the body.

8. (CURRENTLY AMENDED) A method of forming a semiconductor device having a semiconductor body ~~(22)~~ comprising an active area ~~(7)~~ and a termination structure ~~(16)~~ surrounding the active area, the termination structure comprising a plurality of lateral trench-gate transistor devices ~~(2a to 2d)~~ connected in series and extending from the active area towards a peripheral edge ~~(42)~~ of the semiconductor body, each lateral device comprising a trench ~~(30)~~ having a gate electrode ~~(31)~~ therein separated from the semiconductor body by a layer of gate insulating material ~~(32)~~, the gate electrodes of the lateral devices extending through a region of a first conductivity type ~~(15)~~, and part way through an underlying region ~~(14a)~~ of a second, opposite conductivity type, with each lateral device including an electrically conductive connection ~~(8,23)~~ between its gate electrode ~~(31)~~ and the first conductivity type region ~~(15)~~ at the side of the lateral device closer to the active area, such that a voltage difference between the active area ~~(7)~~ and the peripheral edge ~~(42)~~ is distributed across the lateral devices, the method comprising forming the trenches ~~(30)~~, gate electrodes ~~(31)~~ and layers of gate insulating material ~~(32)~~ of the lateral devices in the same respective process steps as trenches ~~(20)~~, insulated electrodes ~~(11)~~ therein and layers ~~(25)~~ of material insulating the insulated electrodes of devices in the active area ~~(7)~~.

9. (CURRENTLY AMENDED) A method of Claim 8 comprising forming a region ~~(15)~~ of the first conductivity type in devices of the active area ~~(7)~~ in the same process step as the first conductivity type region ~~(15)~~ of the lateral devices.